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Docket: 0756-1653

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

in re PATENT application of)	
SHUNPEI YAMAZAKI et al)	
Serial No. 08/818,884)	Group Art Unit: 2871
Filed: 03/17/1997)	Examiner: D. T. NGUYEN
For: ELECTRO-OPTICAL DEVICE AND)	CERTIFICATE OF MAILING
METHOD FOR MANUFACTURING THE)	thereby certify that this
SAME)	the United States Rootel Constitution
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		missioner for Patents, P.O. Box 1450 Alexandria, M. 22313-1450 on (a-2-a-b)

Honorable Assistant Commissioner of Patents Washington, D.C. 20231

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing references known to Applicant and requests that these references be made of record in the above identified application. Copies of the references listed are submitted herewith in accordance with 37 C.F.R. 1.98(a).

INFORMATION DISCLOSURE STATEMENT

In accordance with 37 C.F.R. § 1.97(e), it is certified that either (1) each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement, or (2) no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign patent application and no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this information disclosure statement.

JP 63-208896 discloses a thin film transistor which comprises a lower gate electrode (2); a lower gate insulating film (3); a semiconductor layer for forming a

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channel (4); a pair of semiconductor layers which are doped with an impurity and function as a source and a drain (5), an upper gate insulating film (6); and an upper gate electrode (12), wherein the lower and the upper gate electrodes (2 and 12) comprises a light shielding conductive material, and wherein a lower gate wiring (2') which is an extended portion of the lower gate electrode (2) and an upper gate wiring (12') which is an extended portion of the upper gate electrode (12) are electrically connected with each other in a portion other than the thin film transistor.

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The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280. A duplicate copy of this sheet is attached.

Respectfully submitted,

Eric J. Robinson

Reg. No. 38,285

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^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

¹ Unique citation designation number. ² Applicant is to place a check mark here if English language Translation is attached.